What is claimed is:

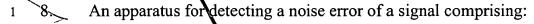
An apparatus for detecting a noise error of a signal comprising:

- a high comparator that references a high voltage limit with the signal and
- 3 generates an output;
- a low comparator that references a low voltage limit with the signal and
- 5 generates an output; and
- a circuit that processes the high comparator output and the low comparator
- output, wherein the circuit generates an alarm if a noise error is detected.
- 1 2. The apparatus of claim 1, wherein the circuit comprises:
- a high-to-low sub-circuit that detects a noise error during a rising signal
- 3 transition; and
- a low-to-high sub-circuit that detects a hoise error during a falling signal
- 5 transition.
- 1 3. The apparatus of claim 2, wherein the high to-low sub-circuit and the low-
- 2 to-high sub-circuit each comprise:
- a plurality of flip-flop circuits;
- a delay buffer; and
- 5 an XOR logic gate.
- 1 4. The apparatus of claim 1, wherein the high comparator and the low
- 2 comparator each comprise a differential amplifier.

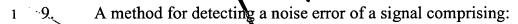
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- 1 5. The apparatus of claim 1, wherein the high comparator and the low comparator each comprise a sense amplifier.
- 1 6. The apparatus of claim 1, wherein the difference between the high voltage
- 2 limit and the low voltage limit is 300 mV.
- An apparatus for detecting a noise error of a signal comprising:
- a high comparator that references a high voltage limit with the signal and generates an output;
  - a low comparator that references a low voltage limit with the signal and generates an output, wherein the difference between the high voltage limit and the low voltage limit is 300 mV;
- a high-to-low sub-circuit that detects a noise error during a rising signal transition, wherein the high-to-low sub-circuit comprises,
- 9 a plurality of flip-flop circuits;
- a delay buffer; and
- an XOR logic gate;
- a low-to-high sub-circuit that detects a noise error during a falling signal transition, wherein the low-to-high sub-circuit comprises,;
- a plurality of flip-flop circuits;
- a delay buffer; and
- an XOR logic gate; and
- wherein either sub-circuit generates an alarm if a noise error is detected



- 2 means for detecting a high voltage noise error;
- means for detecting a low voltage noise error; and
- 4 means for activating an alarm signal upon detection of the high voltage or
- 5 the low voltage noise error.



- comparing a high signal voltage with a high voltage limit;
- activating an alarm if the high signal voltage is less than the high voltage
- 4 limit;
- 5 comparing a low signal voltage with a low voltage limit; and
- activating an alarm if the low signal voltage is greater than the low voltage
- 7 limit.
- 1 10. The method of claim 9, wherein the difference between the high voltage
- 2 limit and the low voltage limit is 300 mV.
- 1 11. The method of claim 9, wherein the low signal voltage is compared with
- 2 the low voltage limit by a low-to-high sub-circuit that detects the noise error
- during a falling signal transition, wherein the low-to-high sub-circuit comprises,
- a plurality of flip-flop circuits;
- 5 a delay buffer; and
- 6 an XOR logic gate.

limit.

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1	12. The method of claim 9, wherein the high signal voltage is compared w	1th
2	the high voltage limit by a high-to-low sub-circuit that detects the noise error	
3	during a falling signal transition, wherein the low-to-high sub-circuit compris	ses,
4	a plurality of flip-flop circuits;	
5	a delay buffer; and	
6	an XOR logic gate.	
1	13 A method for detecting a noise error of a signal comprising:	
2	comparing a high signal voltage with a high voltage limit using a high	-to-
3	low sub-circuit that detects the noise error during a falling signal transition,	
4	wherein the low-to-high sub-circuit comprises,	
5	a plurality of flip-flop circuits,	
6	a delay buffer, and	
7	an XOR logic gate;	
8	activating an alarm if the high signal voltage is less than the high voltage	ıge
9	limit;	
10	comparing a low signal voltage with a low voltage limit using a low-to-	-high
11	sub-circuit that detects the noise error during a falling signal transition, where	ein
12	the low-to-high sub-circuit comprises,	
13	a plurality of flip-flop circuits,	
14	a delay buffer, and	
15	an XOR logic gate; and	
16	activating an alarm if the low signal voltage is greater than the low vo	ltage